50 nm Vertical Replacement-Gate (VRG) pMOSFETs

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Abstract

We present the first p-channel Vertical Replacement-Gate (VRG) MOSFETs. Like the VRG-nMOSFETs demonstrated last year (1), these devices show promise as a successor to planar MOSFETs for highly-scaled ULSI. Our pMOSFETs retain the key features of the nMOSFETs and add channel doping by ion implantation and raised source/drain *extensions* (SDEs). We have significantly improved the core VRG process to provide high-performance devices with gate lengths of 100 nm and below. Since both sides of the device pillar drive in parallel, the drive current per μm of coded width can far exceed that of planar MOSFETs. Our 100 nm VRG-pMOSFETs with t_{OX} = 25 Å drive 615 μA/μm at 1.5 V with I_{OFF} = 8 nA/μm – 80% more drive than specified in the 1999 ITRS Roadmap at the same I_{OFF}. We demonstrate 50 nm VRG-pMOSFETs with t_{OX} = 25 Å that approach the 1.0 V roadmap target of I_{ON} = 350 μA/μm at I_{OFF} = 20 nA/μm without the need for a hyperthin (< 20 Å) gate oxide.

Introduction

Last year, we demonstrated the first VRG-nMOSFETs, unique devices aimed at high-performance logic and memory applications (1). In this paper, we present the first p-channel VRG-MOSFETs. As in the original nMOSFETs, these devices feature 1) control of *all* critical dimensions without lithography, 2) a high-quality gate oxide grown on a single-crystal silicon channel, 3) self-aligned SDEs formed by solid source diffusion (SSD), 4) low parasitic overlap and junction capacitances, and 5) a replacement-gate approach to enable alternative gate stacks. On top of this unique combination, the VRG-pMOSFETs discussed here add: 1) channel doping by ion implantation [a critical enabler for VRG-CMOS (2), precise V_T control, and vertical channel engineering] and 2) raised source/drain *extensions* for improved overall performance. We have also significantly enhanced the core VRG process by reducing the thermal budget for the channel growth step [allowing us to drive SSD by rapid thermal anneal (RTA)], and by improving gate oxide processing and SDE engineering. These enhancements enable the fabrication of high-performance short-channel VRG-pMOSFETs.

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Device Fabrication

The VRG process is significantly different than all previous flows used to fabricate vertical MOSFETs (3-6). The flow used to realize VRG-pMOSFETs is shown in Fig. 1. A multilayer stack of borosilicate glass (BSG)/nitride/undoped oxide/nitride/BSG/nitride is deposited on top of a boron-doped source layer and a rectangular trench (or cylindrical window) is etched through the entire stack. The undoped oxide film in this stack is a sacrificial layer whose thickness defines the gate length L_G. A well-controlled etch in 200:1 HF is used to create 150 or 250 Å recesses in the BSG layers, leading to raised SDEs in the final structure. An undoped epitaxial Si device channel is grown selectively in this trench. Excellent crystalline quality, selectivity, and reproducibility (Fig. 2) were achieved by careful surface preparation to remove trench etch damage, surface contaminants, and native oxide. After the channel is planarized to the top nitride layer by CMP, the device channel is uniformly doped by a series of phosphorus implants. A subsequent RTA with a negligible thermal budget prevents potentially disastrous transient-enhanced diffusion during the subsequent deposition and oxidation steps. A polysilicon drain landing pad is deposited, implanted, and patterned. After this landing pad and the top BSG dopant source have been encased in nitride, the sacrificial oxide layer is removed selectively to expose the sidewalls of the vertical Si channel. A thin gate oxide is grown on the channel, and an in-situ boron doped, highly conformal a-Si gate is then deposited and recrystallized. The gate is patterned and backend processing is carried out. Note that the RTA which drives SSD to form the SDEs is performed before gate oxidation to prevent boron penetration and to enable the possible future use of high-temperature intolerant, alternative gate stacks.

Fig. 3 shows SIMS profiles of boron SSD from highly doped, blanket BSG dopant sources for different RTA conditions. Solid-solubility limited, steep (9 nm/dec) junctions with competitive sheet resistances were obtained (7). SSD results such as these were used to calibrate 2D process simulations. The final doping geometry simulated for a typical 100 nm VRG-pMOSFET is shown in Fig. 4. The scanning capacitance image of Fig. 5 qualitatively illustrates the

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doping geometry in a 200 nm device. The extraction of quantitative information about channel lengths and junction depths from images like this is an area of active research. The TEM image of Fig. 6(a) shows a completed 50 nm VRG-pMOSFET with an epi-Si channel exhibiting perfect crystal quality and a 32 Å (measured by TEM) gate oxide. This image also illustrates a self-aligned, recessed channel created before gate oxidation and the raised SDEs. Figures 6(b) and (c) show blow-ups of the active region and the 32 Å gate oxide. The gate oxide does not show the thinning near the edges of the gate previously observed in the VRG geometry.

Device Performance

Fig. 7 shows the planview geometry of a rectangular VRG-MOSFET and defines the coded width W_C. We have estimated (2) that a typical logic layout for VRG CMOS can pack the same density of devices with equivalent coded width as can planar CMOS, so the drive current is appropriately normalized to W_C here. The subthreshold and I_D-V_{DS} characteristics for a VRG-pMOSFET with L_G = 200 nm and t_{OX} = 30 Å (TEM) are shown in Fig. 8. At an operating voltage of 1.8 V, the drive current of this device divided by its coded width W_C is 550 µA/µm with I_{OFF} = 2 nA/µm and subthreshold swing s = 84 mV/decade. The associated I_D-V_{DS} characteristics are well-behaved and show floating-body (kink) effects similar to partially-depleted SOI. The 100 nm VRG-pMOSFET of Fig. 9 has a very high drive current of 615 µA/µm at 1.5 V with I_{OFF} = 8 nA/µm (the 1999 ITRS Roadmap value for 1.5 V high-performance operation). The subthreshold swing s = 85 mV/decade. Fig. 10 shows the I_{ON}-I_{OFF} distribution for $L_G \approx$ 100 nm pMOSFETs with two different channel doping values. All of the devices fall tightly along a single curve, demonstrating the excellent control of the VRG process. The remaining variation along this trend line among nominally identical devices reflects a wafer-scale process non-uniformity whose nature is still under investigation. This variation may well be removed by further process optimization. Fig. 10 also shows the roadmap I_{ON}-I_{OFF} specification for high-performance 1.5 V devices. Despite their conservative 25 Å (TEM) gate oxides, our 100 nm pMOSFETs outdrive this specification by nearly 80%. Fig. 11 shows the subthreshold and I_D-V_{DS} characteristics for a 50 nm VRG-pMOSFET with t_{OX} = 25 Å and V_{DD} = 1.0 V. This device exhibits excellent overall 1.0 V performance with s = 98 mV/decade, I_{ON} = 330 µA/µm and $I_{OFF} \approx$ 20 nA/µm. Fig. 12 indicates that the I_{ON}-I_{OFF} distribution for $L_G \approx$ 50 nm VRG-pMOSFETs approaches the 1.0 V roadmap specification without the need for a hyperthin (< 20 Å) gate oxide. This respectable 1.0 V performance can be significantly improved by decreasing t_{OX}, incorporating thinner nitride offset spacers (*i.e.* moving the BSG dopant sources closer to the gate), and by optimizing the SDE profile and depth.

Future Options

We have chosen to operate in the partially-depleted (PD) regime since this does not require advanced lithography nor is it sensitive to channel thickness variations. PD operation is appropriate as long as it allows continued performance improvement through scaling. Although conventional halos, super-halos, and super-steep retrograde wells are difficult to implement in the VRG process, their absence can be offset by very tight ($3\sigma < 3\%$) L_G control. The new knob of vertical channel engineering (*i.e.* grading the channel doping along its length) may be used to improve short-channel performance and enhance the surface mobility. Although the unique VRG process flow is mechanically scalable to sub-30 nm gate lengths with excellent control, it will be difficult to maintain PD operation and provide electrical scalability to gate lengths this short. However, if one provides a very thin silicon channel (t_{Si}) by advanced lithography or other means, then the VRG process provides a new route to the fabrication of highly-scalable, fully-depleted double-gate MOSFETs with self-aligned gates and well-controlled parasitics.

Conclusions

We have demonstrated the first p-channel VRG-MOSFETs. These devices were built within a CMOS-compatible framework with the channel dopants introduced by ion implantation. The unique VRG process enables the fabrication of high-performance 50 nm devices with ultrathin gate oxides, precise L_G control, raised SDEs and small parasitics. Our 100 nm devices far exceed the 1.5 V roadmap I_{ON}-I_{OFF} targets. We have also demonstrated initial results on high-performance 50 nm VRG-pMOSFETs that are fabricated using current manufacturing methods, materials, and tools, and without advanced lithography.

References

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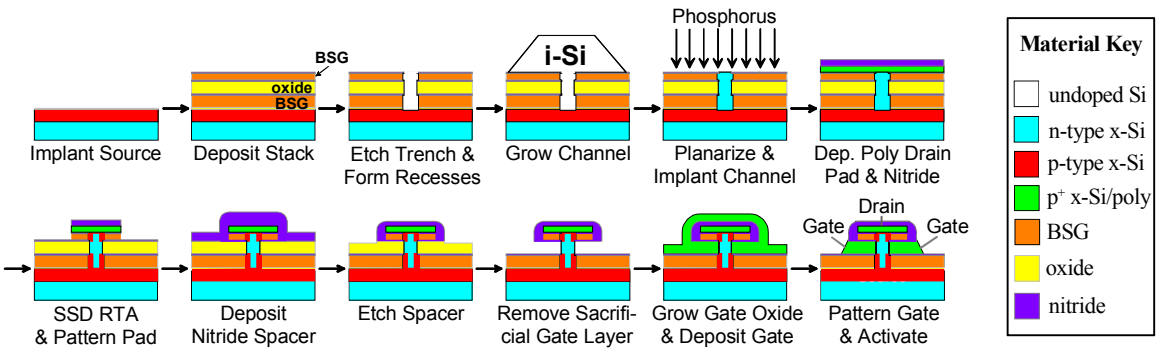

Fig. 1. VRG-pMOSFET front-end process flow incorporating channel doping by ion implantation and elevated source/drain *extensions*.

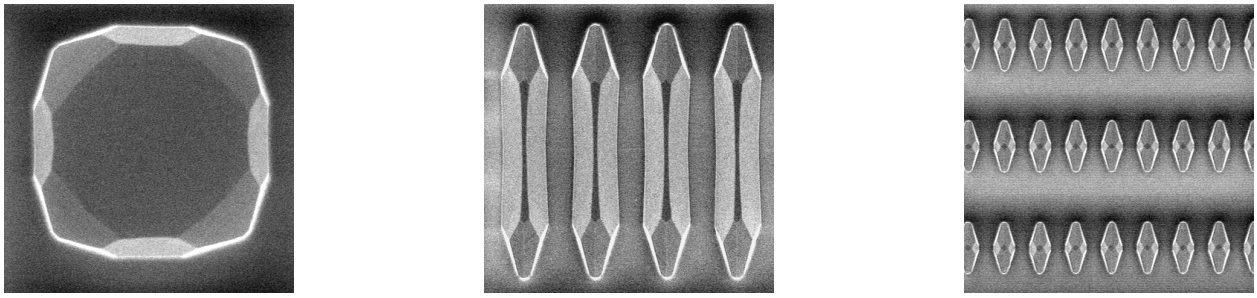

Fig. 2. Top-down SEM images of the selective epitaxial growth of the initially undoped Si device channel in windows and trenches. This growth is perfectly selective and uniform and has excellent crystalline quality. CMP is used to planarize the silicon channel.

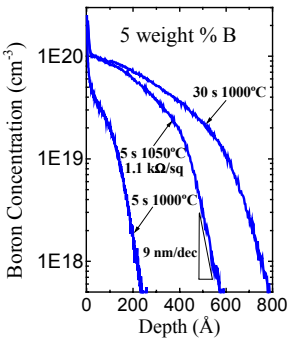

Fig. 3. SIMS profiles of boron SSD driven by RTA. Competitive, solubility-limited profiles with steep gradients were obtained.

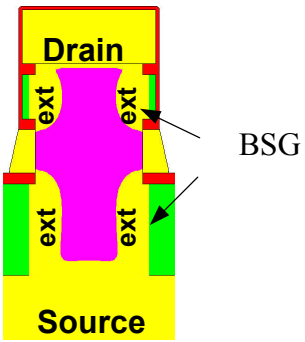

Fig. 4. Final doping geometry of a typical 100 nm VRG-pMOSFET predicted from calibrated 2D process simulations.

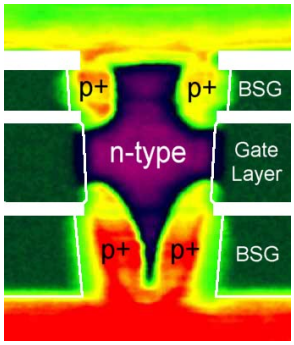

Fig. 5. Scanning capacitance image of a 200 nm VRG-pMOSFET showing the qualitative 2D doping geometry and the n-type channel formed by phosphorus implantation.

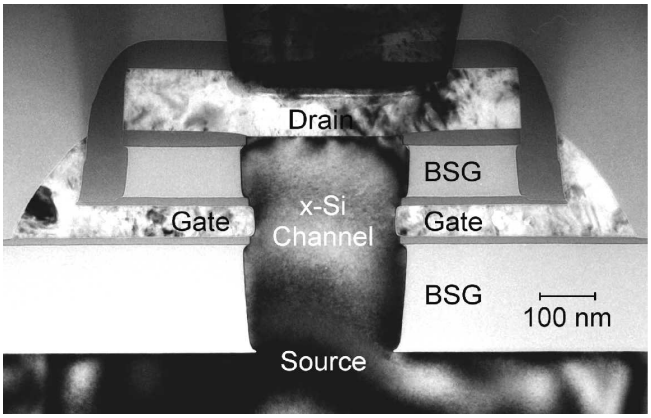

Fig. 6(a) TEM image of a completed 50 nm VRG-pMOSFET showing perfect crystal quality in the channel, elevated SDEs, and gates on either side of the channel.

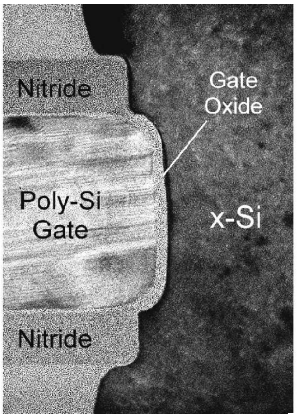

Fig. 6(b) Blow-up of the active area of the device showing the two nitride offset spacers and a recessed-channel structure.

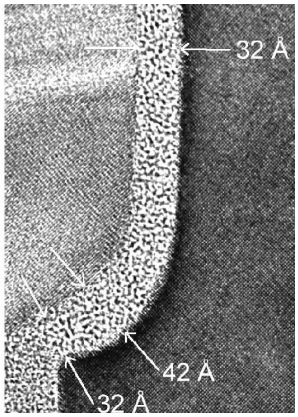

Fig. 6(c) Blow-up of the corner of the gate showing a 32 Å gate oxide without thinning near the gate edges.

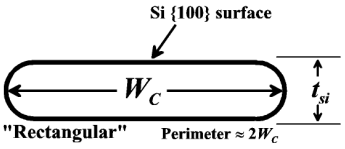

Fig. 7. Planview geometry of the VRG-MOSFET defining the coded width W_C.

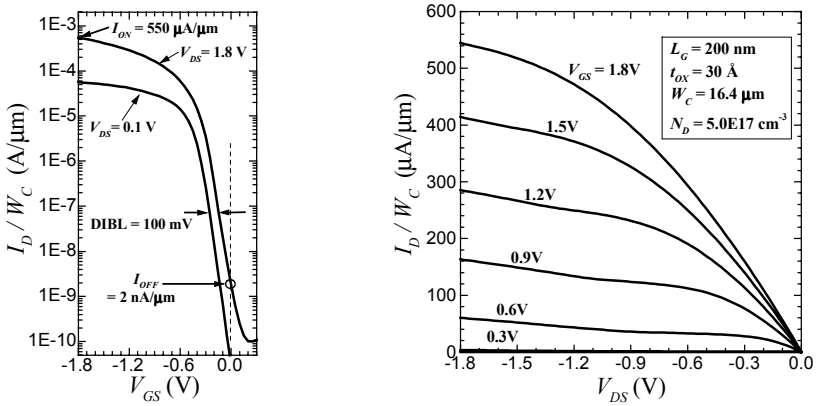

Fig. 8. Subthreshold and I_D-V_{DS} characteristics for a representative L_G = 200 nm VRG-pMOSFET with V_{DD} = 1.8 V. These data are normalized to the coded width W_C (the device perimeter is ≈ $2W_C$). With an I_{OFF} = 2 nA/µm at V_{GS} = 0 V and V_{DS} = 1.8 V, the drive current is 550 µA/µm at V_{GS} = V_{DS} = 1.8 V.

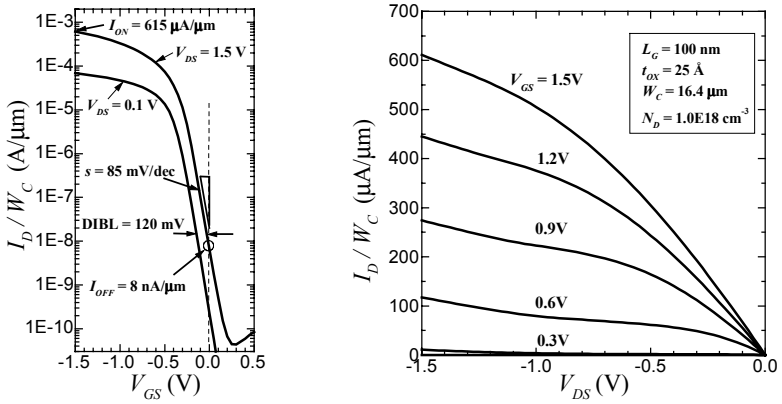

Fig. 9. Subthreshold and I_D-V_{DS} characteristics for a representative L_G = 100 nm VRG-pMOSFET with V_{DD} = 1.5 V. This device has a 1.5 V roadmap target I_{OFF} of 8 nA/µm with a very high drive current of 615 µA/µm.

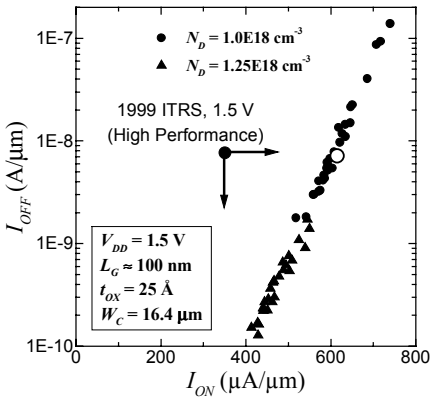

Fig. 10. I_{ON}-I_{OFF} trend for a set of L_G ≈ 100 nm devices far exceeds the 1999 ITRS target for 1.5 V operation. The device of Fig. 9 is indicated by the open circle.

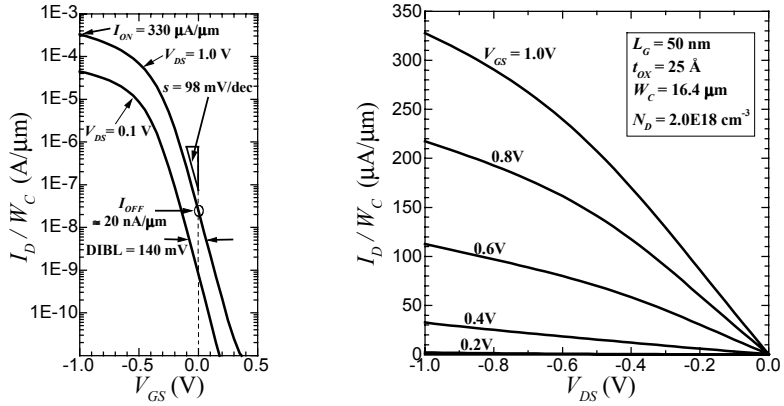

Fig. 11. Subthreshold and I_D-V_{DS} characteristics for a representative L_G = 50 nm VRG-pMOSFET with V_{DD} = 1.0 V. With an I_{OFF} of about 20 nA/µm, this device drives 330 µA/µm.

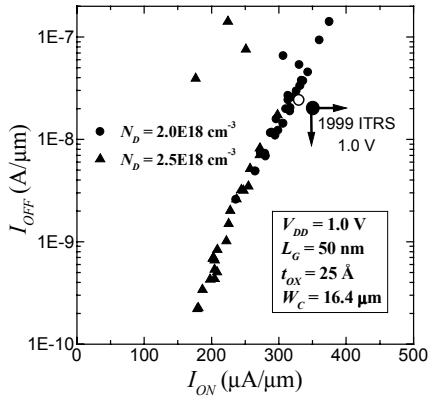

Fig. 12. I_{ON}-I_{OFF} trend for a set of L_G ≈ 50 nm devices approaches the 1999 ITRS target for 1.0 V operation, even with a relatively thick 25 Å (TEM) gate oxide. The device of Fig. 11 is indicated by the open circle.