Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs

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***Abstract*—Short-channel effects in fully-depleted double-gate (DG) and cylindrical, surrounding-gate (Cyl) MOSFETs are governed by the electrostatic potential as confined by the gates, and thus by the device dimensions. The simple but powerful evanescent-mode analysis shows that the length λ, over which the source and drain perturb the channel potential, is $1/\pi$ of the effective device thickness in the double-gate case, and 1/4.810 of the effective diameter in the cylindrical case, in excellent agreement with PADRE device simulations. Thus for equivalent silicon and gate oxide thicknesses, evanescent-mode analysis indicates that Cyl-MOSFETs can be scaled to 35% shorter channel lengths than DG-MOSFETs.**

***Index Terms*—Double-gate MOSFET, MOSFET scaling, short-channel effect, surrounding-gate MOSFET.**

I. Introduction

In CONVENTIONAL bulk MOSFETs, immunity from short-channel effects such as V_T-rolloff and DIBL requires increasing doping to reduce the depletion depth in the substrate. Even when retrograde channel profiles are used to reduce mobility degradation and threshold mismatch, this approach intrinsically trades the improved short-channel immunity for increased substrate-bias sensitivity and degraded long-channel subthreshold swing. However, by replacing the substrate with another gate to form a fully-depleted, double-gate (DG) MOSFET [Fig. 1(a)], short-channel immunity can be achieved with ideal subthreshold swing. When the gate completely surrounds a channel as in the cylindrical, surrounding-gate (Cyl) MOSFET [Fig. 1(b)], the electrostatic control is even better. If the channel doping is uniform, it can be neglected in the short-channel analysis. If we ignore quantum effects that become important for extremely thin (<10 nm) channels, then fully-depleted DG and Cyl devices represent an ideal situation for simple electrostatic analysis. In previous analyses [1], [2], the electrostatic potential ψ in the channel is unjustifiably assumed to be a parabolic function of the transverse position (defined as y for DG and as ρ for Cyl). Then, although the free carriers are irrelevant to the electrostatics, the Laplace equation ($d^2\psi/dx^2 + d^2\psi/dy^2 = 0$ for DG) is solved along the path of the dominant subthreshold current (i.e., at the Si/SiO_2 interface in [1] and at the center of the channel in [2]). The resulting potential decays exponentially along the channel, $\psi(x, y) \propto \exp(\pm x/\lambda)$, where the characteristic length λ depends on the transverse curvature of the potential at the chosen position. Shorter transverse dimensions (i.e., smaller $t_{\rm Si}$ and t_{ox}) lead to shorter values of λ, resulting in better short-channel characteristics. The minimum acceptable channel length $L_{\rm min}$ is between 3λ and 7λ, depending on the magnitude of short-channel effects that can be tolerated and on details of the device doping geometry.

Unfortunately, when the solution is determined at the Si/SiO_2 interface as in [1], the transverse curvature $[(d^2\psi/dy^2)/\psi]$ in the parabolic approximation differs significantly from that of the correct sinusoidal solution, resulting in a severe underestimation of λ for thin gate oxides. In the DG-MOSFET, Yan *et al.* [1] give $\lambda_1 = \sqrt{(\kappa/2)t_{\rm Si}t_{ox}}$, where $\kappa = \varepsilon_{\rm Si}/\varepsilon_{ox} \approx 3$. Suzuki *et al.* [2] who use the same technique but solve Laplace's equation along the center of the DG channel, give $\lambda_2 = \sqrt{(\kappa/2)t_{\rm Si}t_{ox}(1 + t_{\rm Si}/4\kappa t_{ox})}$. λ_1 and λ_2 differ significantly when $t_{ox} < t_{\rm Si}/4\kappa$. λ_2 obtained by Suzuki *et al.* agrees reasonably well with device simulations; however, this agreement is fortuitous because it is only at the channel center that the transverse curvature obtained from the parabolic approximation provides a reasonable estimate of the actual curvature.

II. Evanescent-Mode Analysis and the Double-Gate MOSFET

Evanescent-mode analysis [3]–[6] is a powerful, new method for understanding short-channel effects. It properly deals with the two-dimensional (2-D) nature of the electrostatics and provides qualitatively different scaling predictions than analyses based on the parabolic approximation. Here, we apply it first to the DG-MOSFET. The channel potential is divided into two different pieces, $\psi(x, y) = \psi_L(y) + \psi^*(x, y)$. The long-channel solution ψ_L satisfies the Poisson equation as well as the appropriate gate-bias boundary conditions. Since the doping term in the Poisson equation is taken care of in ψ_L, the short-channel potential ψ^* satisfies the Laplace equation. ψ^* is zero at the Si/SiO_2 interfaces and it must also accommodate the source and drain bias conditions and workfunction differences. In the symmetric DG-MOSFET, ψ^* can be represented as a Fourier expansion of modes, each with its own characteristic decay length, as follows:

$$\psi^*(x, y) = \sum_{n=1}^{\infty} A_n \cos(ny/\lambda) \cdot [B_{n+} \exp(nx/\lambda) + B_{n-} \exp(-nx/\lambda)]. \quad (1)$$

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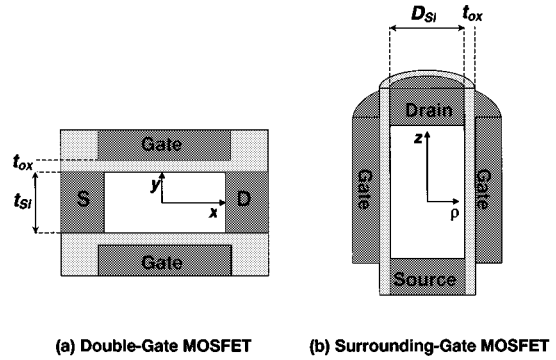

Fig. 1. Cross sections of device structures and coordinates. Double-gate (DG) and cylindrical, surrounding-gate (Cyl) structures are shown. Uniform channel doping and metal-like source/drain regions are used in all simulations.

Woo *et al.* [5] applied this series expansion to fully-depleted SOI devices. Rather than using this long series expansion from which it is difficult to gain critical physical insight, we approximate ψ^* by retaining only the lowest-order mode [3], [4]

$$\psi^*(x, y) \approx A_1 \cos(y/\lambda)\cdot[B_{1+} \exp(x/\lambda)+B_{1-} \exp(-x/\lambda)]. \quad (2)$$

Since the higher order modes decay very quickly, this lowest-mode approximation is very accurate, especially near the channel center. λ is determined by satisfying the boundary conditions that $\psi^* = 0$ at the Si/SiO_2 interfaces, i.e., by fitting a half period of $\cos(y/\lambda)$ between the gate electrodes. If $t_{ox} \ll t_{\rm Si}$, we obtain $\lambda = (t_{\rm Si} + 2\kappa t_{ox})/\pi$, where the oxide is scaled to its effective electrical thickness κt_{ox}. Therefore, *the transverse confinement of the device determines* λ. In the general case of a thicker oxide, we use the electrostatic boundary condition that at each Si/SiO_2 interface, the potential and the component of $\varepsilon\cdot\vec{E}$ perpendicular to the interface should be continuous. This provides an implicit equation for λ [3]

$$\kappa \cdot \tan(t_{\rm Si}/2\lambda) \cdot \tan(t_{ox}/\lambda) = 1. \quad (3)$$

If $t_{ox} \ll t_{\rm Si}$, $\lambda = (t_{\rm Si} + 2\kappa t_{ox})/\pi$ satisfies (3) as expected. Equation (3) was originally derived by Frank *et al.* [3] and its related form applicable in SOI structures was derived by Monroe *et al.*[4].

The evanescent mode is a property of the whole structure rather than just the Si/SiO_2 interface or the channel center, and as such, λ does not depend on transverse position within the channel. We have used the PADRE device simulator [7] to calculate $\psi(x, y)$ and to obtain λ in the following manner. The potential along the channel center for $V_{DS} = 0$ V and 0.1 V is shown in Fig. 2(a). The difference, $\Delta\psi(x, y) = \psi(V_{DS} = 0.1\,\text{V}) - \psi(V_{DS} = 0\,\text{V})$, is shown on a semi-log plot in Fig. 2(b). Since $\Delta\psi \propto \exp(\pm x/\lambda)$, λ can be obtained directly from the slope of the linear region of each curve in Fig. 2(b). As we can clearly see, λ is independent of the transverse position. This is in direct contrast to predictions of other analyses based on the parabolic approximation.

In Fig. 3, we vary t_{ox} and compare λ predicted by each analytic model with the PADRE results. λ from evanescent-mode analysis was calculated by solving (3), and λ from simulation was extracted using the method of Fig. 2(b). The analytic results from evanescent-mode analysis agree extremely well with the PADRE results. Note that in the analysis of Yan *et al.*, $\lambda \to 0$ as

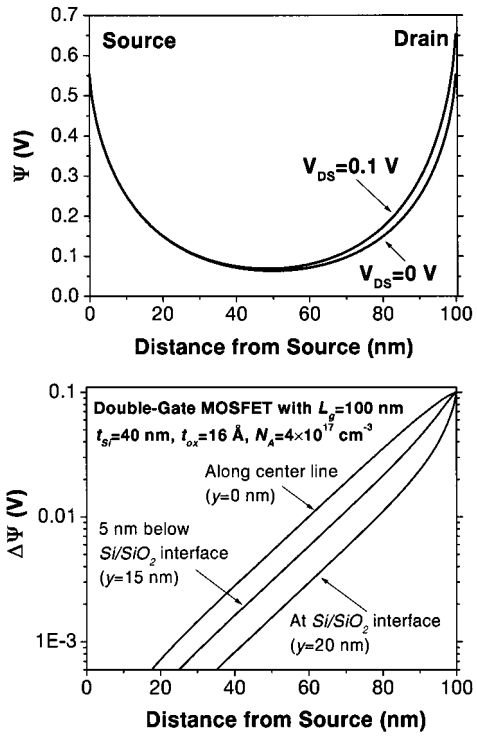

Fig. 2. (a) Potential along the channel of a DG-MOSFET with applied source-drain biases of 0 V and 0.1 V. Parameters used are $L_g = 100$ nm, uniform channel doping of $N_A = 4 \times 10^{17}/\text{cm}^3$, $t_{\rm Si} = 40$ nm, $t_{ox} = 16$ Å, and a 4.17 eV workfunction for the source and drain. The potential is extracted along the Si/SiO_2 interface at $y = t_{\rm Si}/2$. (b) The difference between the channel potential with applied source-drain biases of 0 V and 0.1 V shown on a semi-log plot along lines at three transverse positions in the channel. The equivalent slopes of these lines indicate that the characteristic length λ is independent of transverse position.

$t_{ox} \to 0$. This is *qualitatively* different from evanescent-mode analysis, which indicates that λ is nonzero even as $t_{ox} \to 0$ due to the nonzero thickness of the silicon channel.

III. Application to the Cylindrical, Surrounding-Gate MOSFET

Evanescent-mode analysis was previously applied to device structures such as DG, fully-depleted SOI, and super-steep retrograde bulk [4]. Here, we extend this analysis to the case of the cylindrical, surrounding-gate (Cyl) MOSFET [8] of Fig. 1(b). The channel potential is again divided into two pieces, $\psi_L(\rho)$ and $\psi^*(\rho, z)$, where ψ^* is a solution of the Laplace equation. The general solution of the Laplace equation in cylindrical coordinates with a finite potential at $\rho = 0$ is [9]

$$\psi^*(\rho, \phi, z) = \sum_{m=0}^{\infty}\sum_{n=1}^{\infty} J_m(k_{mn}\rho)\cdot(A_{mn}\cos m\phi + B_{mn}\sin m\phi) \cdot (C_{mn+}e^{k_{mn}z} + C_{mn-}e^{-k_{mn}z}) \quad (4)$$

where J_m is the Bessel function of order m. Keeping only terms with $m = 0$ (since the potential cannot depend on ϕ due to cylindrical symmetry) and defining $\lambda_{\rm Cyl} \equiv 1/k_{01}$, the lowest-order ($n = 1$) mode is given by

$$\psi^*(\rho, z) \approx A_{01}\cdot J_0(\rho/\lambda_{\rm Cyl})\cdot\left(C_{01+}e^{z/\lambda_{\rm Cyl}} + C_{01-}e^{-z/\lambda_{\rm Cyl}}\right). \quad (5)$$

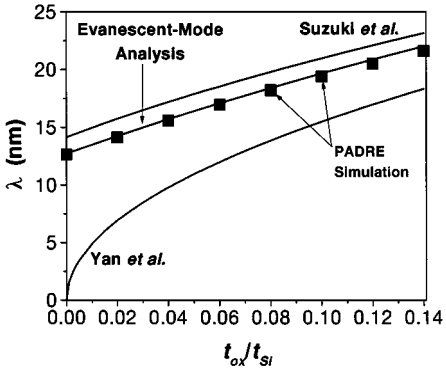

Fig. 3. Comparison of λ from three different analytic models and the results of PADRE simulations using the same L_g, N_A, and $t_{\rm Si}$ of Fig. 2. Evanescent-mode analysis predicts a characteristic length λ that agrees extremely well with PADRE simulations.

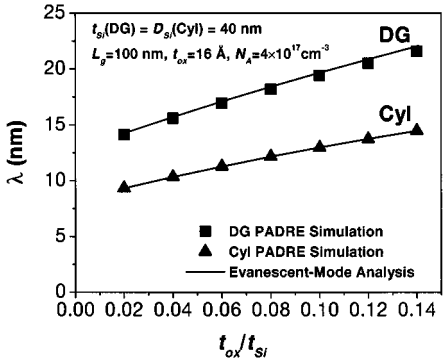

Fig. 4. Comparison of DG- and Cyl-MOSFET results. λ as obtained from evanescent-mode analysis is compared with PADRE simulation results for both DG- and Cyl-MOSFETs and shows excellent agreement.

$\lambda_{\rm Cyl}$ is fixed by fitting the first zero of $J_0(x)$ at the gate electrode located at $\rho = (D_{\rm Si} + 2t_{ox})/2$.

For $t_{ox} \ll D_{\rm Si}$, as in the DG case, the different dielectric constants are taken into account by using the effective electrical oxide thickness κt_{ox}. Since the first zero of $J_0(x)$ occurs at $x = 2.405$, we obtain $\lambda_{\rm Cyl} = (D_{\rm Si} + 2\kappa t_{ox})/4.810$. We now compare this result with that for the DG-MOSFET for the case of $t_{\rm Si} = D_{\rm Si}$ and equivalent t_{ox}. Since $\lambda_{DG} = (t_{\rm Si} + 2\kappa t_{ox})/\pi$, we find that $\lambda_{\rm Cyl} = 0.653\,\lambda_{DG}$. Thus, $\lambda_{\rm Cyl}$ is about 35% smaller than λ_{DG}, assuming the same silicon dimensions, t_{ox}, and doping geometry. This can be understood to result from the tighter confinement present in the Cyl-MOSFET—whereas the DG structure has only one small transverse dimension, the cylindrical structure offers confinement from all transverse directions. This tighter confinement leads to a faster exponential decay of the potential along the channel length. The ratio $\lambda_{\rm Cyl}/\lambda_{DG}$ obtained with evanescent-mode analysis is in reasonable agreement with previous work by Auth and Plummer [10]. However, the Auth–Plummer result is based on the parabolic approximation and is only intended to provide an estimate of λ in the special case in which the dominant subthreshold current occurs at the center of the channel. In contrast, the characteristic length $\lambda_{\rm Cyl}$ determined from evanescent-mode analysis is quite general and has a firm physical basis.

When t_{ox} is not very small, we solve the Laplace equation separately in the silicon and oxide regions. In cylindrical coordinates, the Bessel function $J_0(\rho)$ and the Neumann function $Y_0(\rho)$ are linearly independent solutions of the Laplace equation. The electrostatic boundary condition that the perpendicular component of $\varepsilon \cdot \vec{E}$ is conserved at the Si/SiO_2 interface gives an implicit equation for $\lambda_{\rm Cyl}$, as follows:

$$\frac{Y_0'(D_{\rm Si}/2\lambda_{\rm Cyl})}{J_0'(D_{\rm Si}/2\lambda_{\rm Cyl})} = \kappa \frac{Y_0(D_{\rm Si}/2\lambda_{\rm Cyl})}{J_0(D_{\rm Si}/2\lambda_{\rm Cyl})} + (1-\kappa)\frac{Y_0((D_{\rm Si}+2t_{ox})/2\lambda_{\rm Cyl})}{J_0((D_{\rm Si}+2t_{ox})/2\lambda_{\rm Cyl})}. \quad (6)$$

In Fig. 4, we compare λ for a DG- and a Cyl-MOSFET as a function of t_{ox}. We can clearly see the advantage of the cylindrical structure, which gives a 35% smaller λ compared to the DG structure. We also plot PADRE results which match very well with predictions from evanescent-mode analysis.

IV. Conclusion

Short-channel analyses based on the parabolic approximation provide inaccurate results for the characteristic length λ as well as the electrostatic potential in the channel. Evanescent-mode analysis, which properly deals with the 2-D electrostatic effects, provides solutions which accurately represent the potential in the entire device channel. One of the main physical insights provided by evanescent-mode analysis is that λ is directly related to the *transverse confinement provided by the device*. We have extended this analysis to the cylindrical case, and conclude that when compared to the DG-MOSFET, the tighter confinement from all directions allows the Cyl-MOSFET to be scaled to 35% shorter channel lengths.

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