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The vertical replacement-gate (VRG) MOSFET

J.M. Hergenrother *, Sang-Hyun Oh, T. Nigam, D. Monroe, F.P. Klemens, A. Kornblit

Agere Systems, Room 2D-312B, 600 Mountain Avenue, Murray Hill, NJ 07974, USA

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Abstract

We have fabricated and demonstrated a new device called the vertical replacement-gate (VRG) MOSFET. This is the first MOSFET ever built in which: (1) all critical transistor dimensions are controlled precisely without lithography and dry etch, (2) the gate length is defined by a deposited film thickness, independently of lithography and etch, and (3) a high-quality gate oxide is grown on a single-crystal Si channel. In addition to this unique combination, the VRG-MOSFET includes self-aligned source/drain extensions (SDEs) formed by solid source diffusion (SSD), small parasitic overlap, junction, and source/drain capacitances, and a replacement-gate approach to enable alternative gate stacks. We have demonstrated nMOSFETs with an initial VRG process, and pMOSFETs with a more mature process. Since both sides of the device pillar drive in parallel, the drive current per μm of coded width can far exceed that of advanced planar MOSFETs. Our 100 nm VRG-pMOSFETs with $t_{OX} = 25$ Å drive 615 μA/μm at 1.5 V with $I_{OFF} = 8$ nA/μm—80% more drive than specified in the 1999 ITRS Roadmap at the same I_{OFF}. Our 50 nm VRG-pMOSFETs with $t_{OX} = 25$ Å approach the 1.0 V roadmap target of $I_{ON} = 350$ μA/μm at $I_{OFF} = 20$ nA/μm without the need for a hyperthin (<20 Å) gate oxide. We have described a process for integrating n-channel and p-channel VRG-MOSFETs to form side-by-side CMOS that retains the key VRG advantages while providing packing density and process complexity that is competitive with traditional planar CMOS. *All of this is achieved using current manufacturing methods*, *materials*, *and tools*, and high-performance devices with 50 nm physical gate lengths (L_G) have been demonstrated with precise gate length control without advanced lithography. © 2002 Published by Elsevier Science Ltd.

Keywords: MOSFET; Vertical MOSFET; Replacement-gate; Non-lithographic; Lithography-independent; Solid source diffusion

1. Introduction

The possible benefits of building vertical MOSFETs on the sidewalls of trenches or Si pillars have been recognized for at least a quarter century [1]. Prominent among these benefits is a higher drive current per unit area of Si, the stacking of transistors and storage capacitors, and control of the gate and/or channel length without lithography. Many approaches [1–10] have been used to build these devices, but all vertical MOSFETs have lacked at least one of the following essential characteristics of the advanced planar transistor: high-quality gate oxide, sufficient gate length control, self-aligned source/drain, and low parasitic capacitances. We have demonstrated a new device called the vertical replacement-gate (VRG) MOSFET [11–13] that retains these important planar MOSFET features, and in addition, provides precise critical dimension control without lithography, enhanced performance, and promising new opportunities for device design and continued scaling. In contrast to most vertical MOSFETs, the VRG-MOSFET is aimed not only at memory applications

* Corresponding author. Tel.: +1-908-582-3298; fax: +1-908-582-6000.

E-mail address: jackh@agere.com (J.M. Hergenrother).

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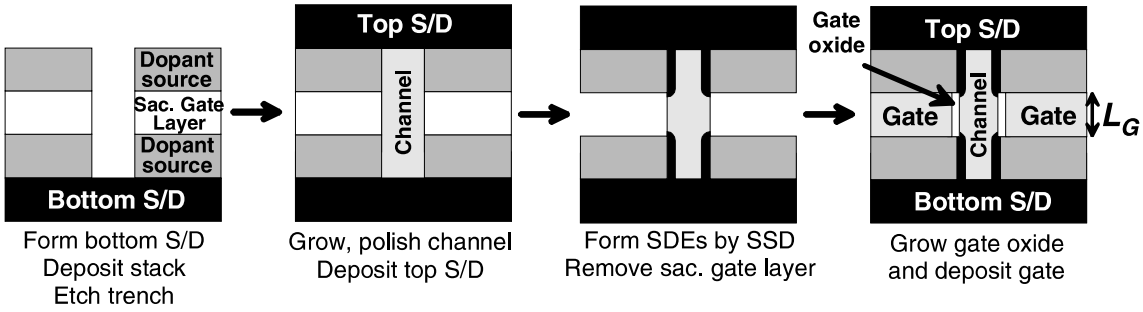

Fig. 1. Outline of the VRG process.

but also at high-performance random logic and high-speed applications.

2. Basic VRG process

The basic ideas of the VRG process are illustrated in Fig. 1. A multilayer stack that contains a sacrificial gate layer and two dopant source layers is deposited. A trench is etched through this stack and it is filled with single-crystal Si to form the device channel. Shallow, self-aligned source-drain extensions (SDEs) are formed by solid source diffusion (SSD) from the dopant sources. The sacrificial gate layer is subsequently removed, a gate oxide is grown on the exposed portion of the channel, and the gate is deposited in place of the sacrificial layer. The key enabling element of the VRG process is its replacement-gate approach—this allows for the fabrication of high-quality gate oxides on a vertical {1 0 0} Si surface whose length is defined by a film thickness. This flow should be mechanically scalable to sub-30 nm gate lengths with excellent ($3\sigma < 3\%$) control. Table 1 summarizes the important features of the VRG process along with some of the promising device design opportunities that it creates.

Table 1
Summary of important VRG process and device features

- All critical dimensions controlled precisely without lithography and dry etch
- Gate length controlled by film thickness
- High-quality gate oxide grown on epi Si channel
- Self-aligned SDEs formed by SSD
- SOI-like parasitic capacitances
- Replacement-gate enables alternative gate stacks
- Device free from substrate—increases design flexibility
- Epi channel plus CMP opens door to 3D integration
- Vertical design enables graded channel doping
- Offset spacers controlled by film thicknesses
- Short-channel performance independent of deep source/drain depths
- Made with production tools, methods, materials

3. Solid source diffusion

Since the vertical VRG geometry precludes the use of ion implantation in the formation of self-aligned SDEs, SSD is another key enabling element of the VRG process. SSD allows us to form self-aligned SDEs in this novel geometry, and it therefore transforms the precise gate length control afforded by the VRG process into precise, lithography-independent channel length control. In the SSD technique, dopants from highly doped phosphosilicate glass (PSG) or borosilicate glass (BSG) diffuse into adjacent silicon to form self-aligned, shallow SDEs. Several groups have demonstrated competitive planar MOSFETs with ultrashallow junctions formed by SSD [14–17]. The dopant concentration in the silicon is determined by its concentration in the oxide, the dopant diffusivity in the oxide as well as in the silicon, the segregation at the interface, and the character of the interface. We can obtain shallow junctions with low sheet resistances using SSD without having to concern ourselves with channeling effects and TED associated with implant damage.

Fig. 2 shows 1-dimensional SIMS profiles of phosphorus SSD driven by rapid thermal anneal (RTA). Blanket PSG films with 4 wt.% phosphorus (1.8×10^{21} P atoms/cm^3) were deposited by PECVD at 400 °C using TEOS, O_2, and trimethyl phosphine on an initially hydrogen terminated {1 0 0} silicon surface. The wafers were subsequently annealed at either 1000 or 1050 °C to form shallow n+ junctions. Although these profiles represent respectable n+ junctions, the surface concentrations do not show a solubility-limited value. This may be due to: (1) interface effects that could be specific to these 1-dimensional, blanket-wafer SSD experiments, or (2) the depletion of phosphorus in the doped oxide near the interface due to the relatively slow diffusion of phosphorus in the oxide. More experiments and modeling work are under way to improve the surface concentration and junction profiles for these n+ junctions.

Fig. 3 shows SIMS profiles of boron SSD from highly doped (5 wt.% boron), blanket BSG dopant sources for different RTA conditions. In contrast to the n+

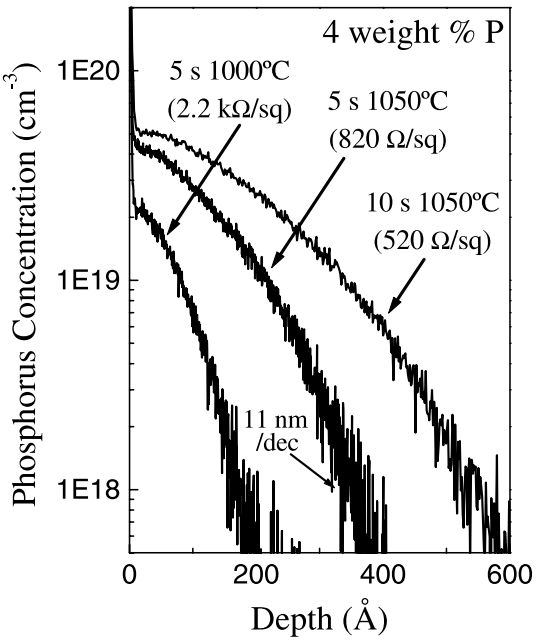

Fig. 2. SIMS profiles of phosphorus SSD driven by RTA.

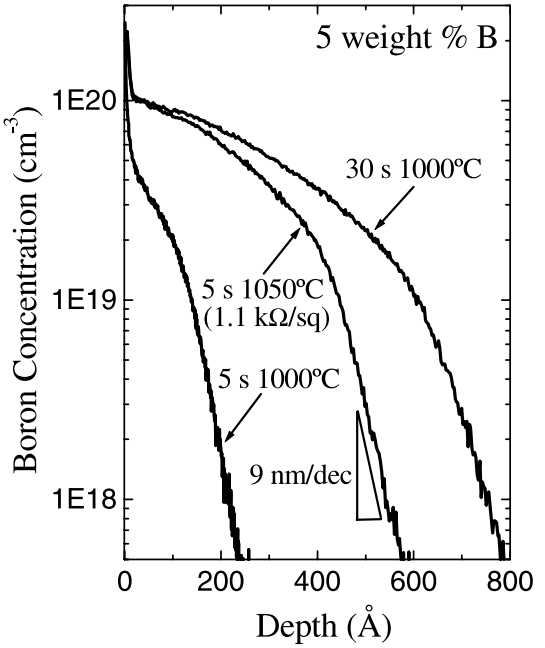

Fig. 3. SIMS profiles of boron SSD driven by RTA. Competitive, solubility-limited profiles with steep gradients were obtained.

junctions of Fig. 2, these profiles represent competitive, shallow p+ junctions. For boron SSD, we have obtained solid-solubility limited, steep (9 nm/dec), box-like junctions with low sheet resistances.

4. Device fabrication of initial VRG-nMOS

The VRG process was first demonstrated with n-channel devices [11]. The process used to fabricate these nMOSFETS is shown in Fig. 4. Arsenic was implanted into an epi Si wafer to form the device drain and a thin oxide diffusion barrier was deposited. A PSG/nitride/undoped oxide/nitride/PSG/nitride stack was deposited and a trench (or window) with nearly vertical sidewalls was etched through the entire stack (Fig. 5). The in-situ boron-doped epitaxial Si device channel was grown selectively in this trench (Figs. 6 and 7) by RTCVD at 850 °C using dichlorosilane and HCl. The growth time was chosen so that the trenches were completely filled (i.e. there was epitaxial lateral overgrowth around the entire perimeter of the trench). The channel was then planarized to the top nitride layer by CMP (Fig. 8). The undoped oxide film in the stack was a sacrificial layer whose thickness defined the gate length L_G, the two PSG layers were dopant sources used to form low-resistance, shallow, self-aligned SDEs by SSD of phosphorus. The phosphorus concentration in these PSG layers was 4 wt.%. The thin nitride layers between the undoped oxide and the dopant sources functioned as

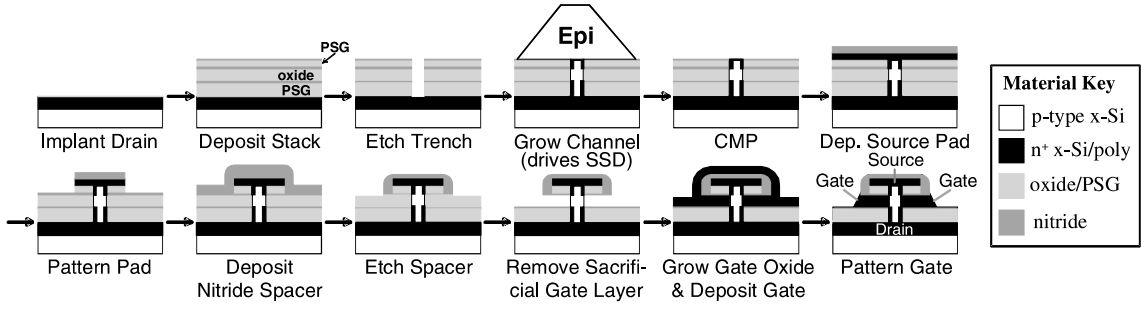

Fig. 4. Process flow used to fabricate the initial VRG-nMOSFETs.

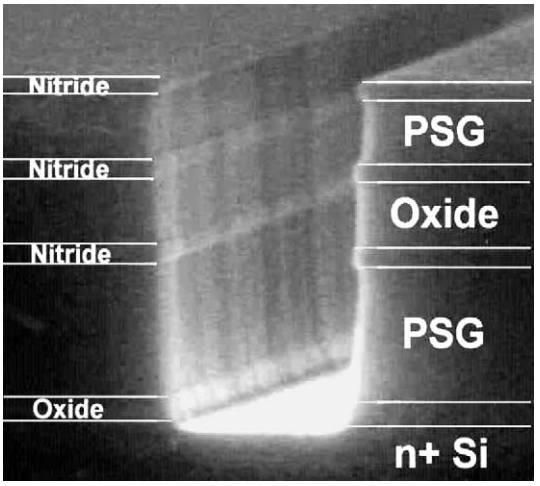

Fig. 5. SEM image of a 0.24 μm trench etched in the oxide/nitride stack.

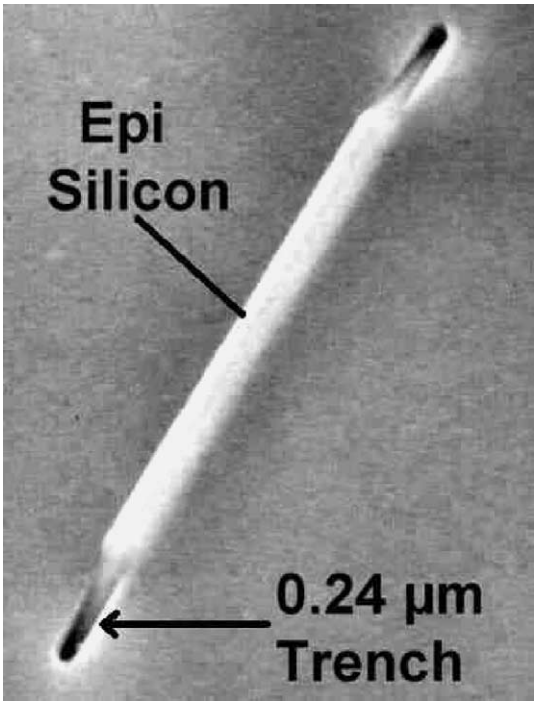

Fig. 6. Birds's eye SEM image of selective epitaxial growth of the device channel (not yet complete).

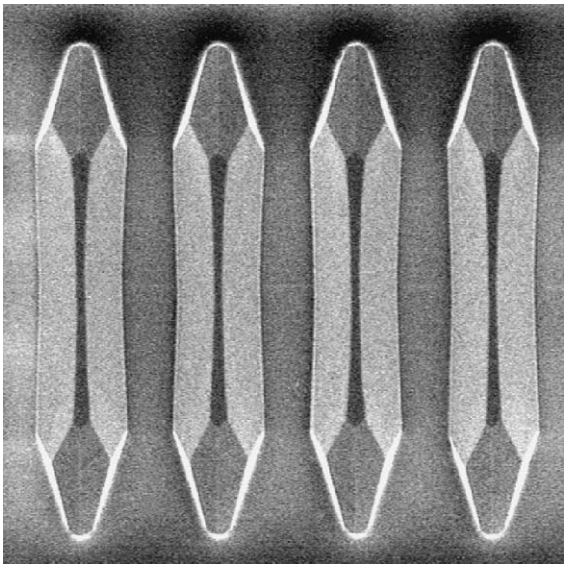

Fig. 7. Top-down SEM image of the completed selective epitaxial growth out of four adjacent trenches. This growth is perfectly selective and uniform and has excellent crystalline quality.

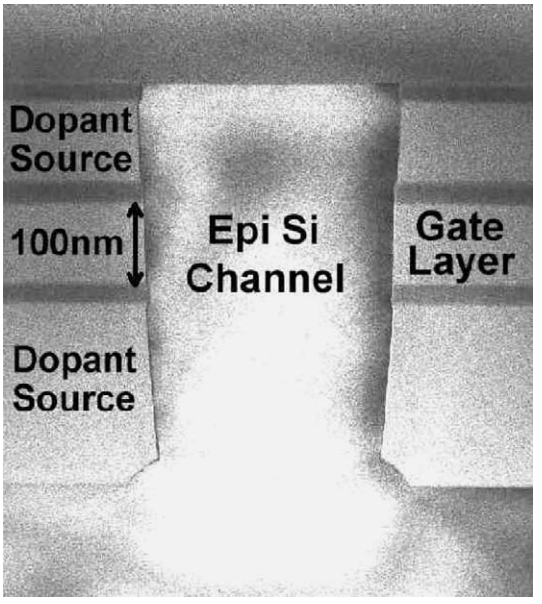

Fig. 8. TEM image of a 100 nm VRG-MOSFET after channel growth and Si CMP.

etch stops and as precision offset spacers. In the completed structure, these nitride offset spacers separated the dopant sources from the polysilicon gate.

After the channel CMP was completed, a polysilicon source landing pad was deposited, implanted with arsenic, and patterned. After this landing pad and the top PSG dopant source had been completely encased in nitride via spacer formation, the sacrificial oxide layer was removed selectively by buffered HF to expose the vertical Si channel (Fig. 9). A thin gate oxide was grown on the channel, and a phosphorous-doped, highly conformal a-Si gate was deposited and recrystallized. The

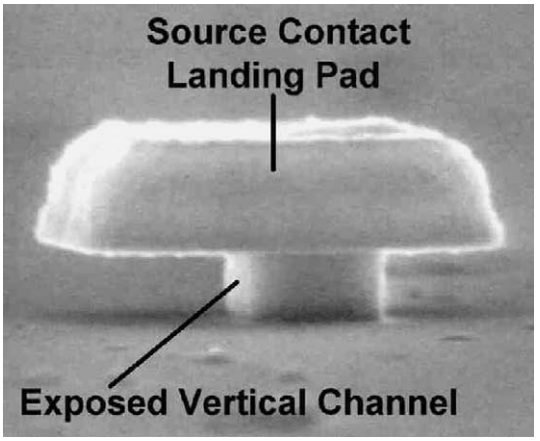

Fig. 9. SEM image of an $L_G = 200$ nm device immediately after the sacrificial gate layer has been removed by buffered HF.

TEM images of Fig. 10(a) and (b) show that the nearly perfect conformality of the a-Si deposition allowed it to fill the space underneath the top of the device without forming voids in the gate. The gate was patterned and backend processing was carried out. In this first demonstration, the SSD occurred almost entirely during the 850 °C selective epitaxial growth of the channel. As we will describe below, we have since been able to reduce the channel growth temperature to 800 °C while maintaining all of the required characteristics. At this reduced temperature, there is negligible SSD of phosphorus (nMOS) or boron (pMOS) during the channel growth step.

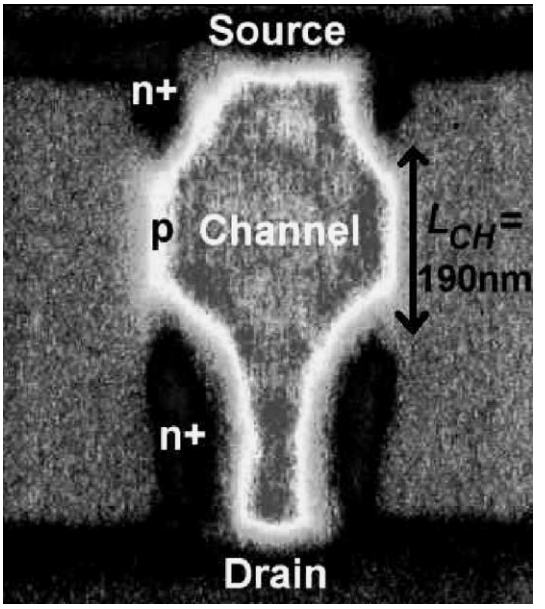

Fig. 11. Scanning capacitance image of an $L_G = 200$ nm VRG-nMOSFET showing self-aligned source/drain extensions.

The VRG-nMOSFET doping geometry was studied by scanning capacitance microscopy [18]. The vertical, self-aligned SDEs are clearly visible in the images of Figs. 11 and 12. In the VRG process, the SDE lengths, as well as their overlaps with the gate, are controlled by film thicknesses. This allows one to precisely tune the overlap capacitances, and consequently, the capacitance/series resistance tradeoff can be optimized asymmetrically for

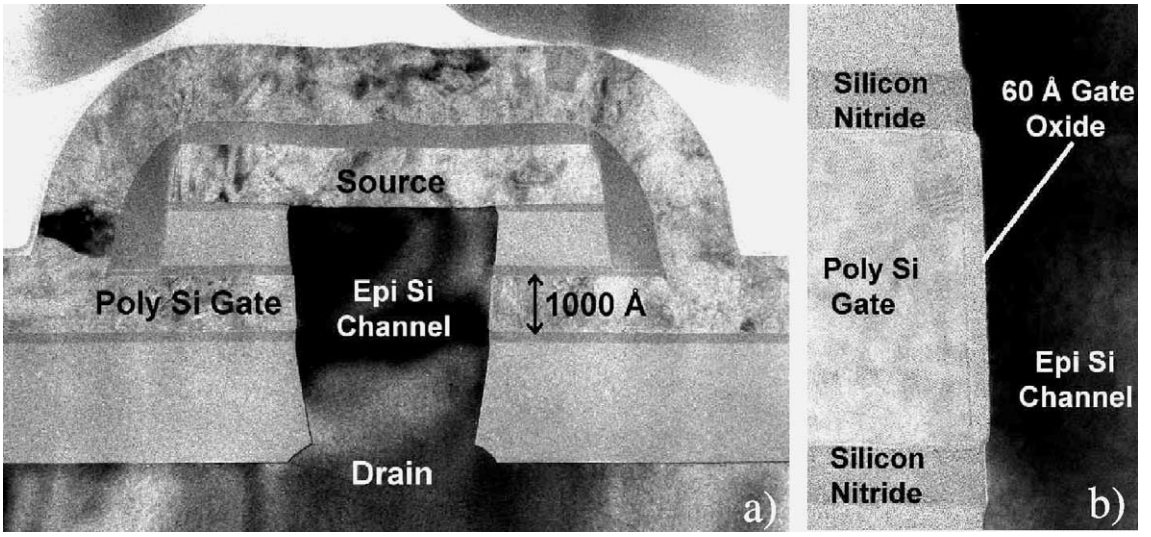

Fig. 10. (a) TEM image of a 100 nm VRG-MOSFET just before gate etch and (b) a blow-up of the channel region showing the polysilicon gate, the two nitride etch stops/offset spacers, and a conservative 60 Å gate oxide.

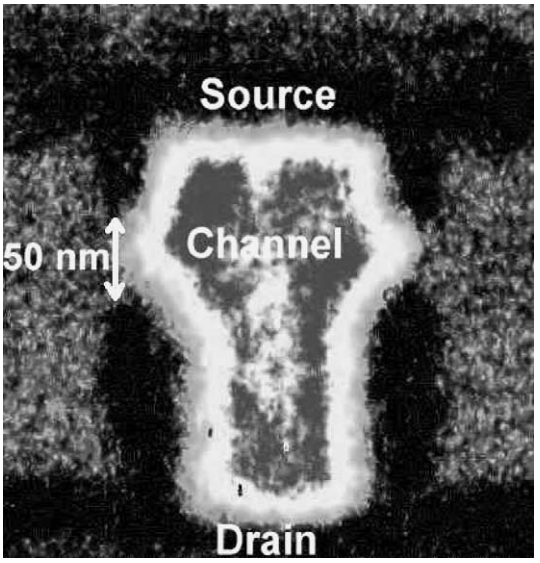

Fig. 12. Scanning capacitance image of an $L_G = 50$ nm VRG-nMOSFET. The two sides of the Si pillar drive in parallel.

the SDEs. In certain applications, it may be advantageous to designate the top electrode as the device drain because of its very low substrate capacitance.

5. Electrical performance of initial VRG-nMOS

In addition to providing precise gate length control and new device design opportunities, the VRG process improves upon the performance of advanced planar

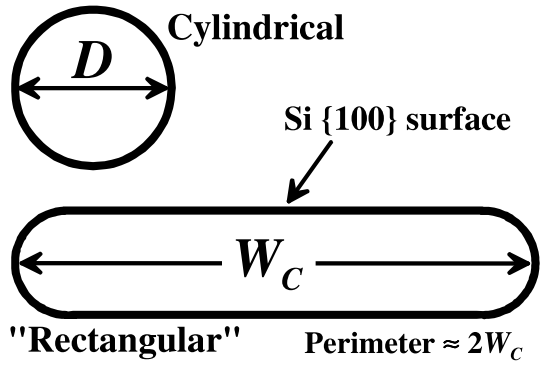

Fig. 13. Planview geometry of two classes of VRG-MOSFETs.

MOSFETs. The subthreshold and I_D–V_{DS} characteristics for a "rectangular" VRG-nMOSFET (see Fig. 13) with $L_G = 200$ nm are shown in Fig. 14. This device is a high-performance MOSFET with a 28 Å physical gate oxide thickness and $V_T = 0.25$ V. At an operating voltage of 2.5 V, the drive current of this device normalized by its coded width W_C is 1.1 mA/μm—about 20% higher than that obtained at 2.5 V for a planar MOSFET with the same L_{CH}, t_{OX}, and $I_{OFF} = 11$ pA/μm at $V_{GS} = V_T - 0.5$ V. We have estimated [12] that a typical logic layout for VRG CMOS can pack the same density of devices with equivalent coded width as can planar CMOS, so the normalization of drive current to W_C is one reasonable metric by which to gauge device performance. The subthreshold swing $s = 76$ mV/decade, which is close to the ideal value (74 mV/decade) for a partially depleted device with $t_{OX} = 28$ Å and $N_A = 5 \times 10^{17}/\text{cm}^3$. The

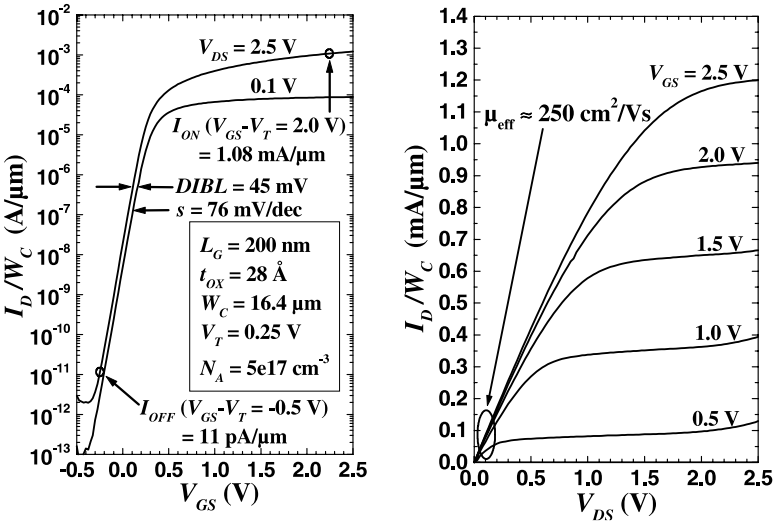

Fig. 14. Subthreshold and I_D–V_{DS} characteristics of a rectangular, $L_G = 200$ nm VRG-nMOSFET with a 28 Å gate oxide. The drive current of this device is a sizeable 1.1 mA/μm at a low I_{OFF} of 11 pA/μm, surpassing the drive of a planar MOSFET with the same L_{CH}, t_{OX}, and I_{OFF}.

saturation transconductance $g_{m,sat} = 540$ μS/μm, and at low V_{DS}, $\mu_{eff} \approx 250$ cm^2/Vs. CV measurements on very wide devices (yield testers with $W_C = 20560$ μm) indicate that the interface trap density at midgap is less than 5×10/cm^2 eV. Straightforward improvements in series resistance and oxide processing (see below) have allowed us to approach the ideal two-fold drive enhancement obtained from having MOSFETs on both sides of the pillar. Note that in our initial nMOS devices, floating body effects are minimal because the device body is unintentionally tied to the source via a leaky junction; this junction is leaky because its depletion region extends to the polysilicon/epi Si interface.

The 50 nm VRG-MOSFET of Fig. 15 also exhibits respectable short-channel performance at 1.5 V with DIBL = 90 mV, $s = 105$ mV/decade, and $I_{OFF} = 13$ nA/μm at $V_{GS} = V_T - 0.4$ V. This 50 nm nMOSFET was far from optimized—it suffered from three important problems that limited its I_{ON} to a relatively low 180 μA/μm at 1.5 V: (1) the dry oxidation recipe used to grow the gate oxide produced a significantly non-uniform oxide in the VRG geometry, leaving it quite *thick* (≈65 Å) for 10–15 nm from each edge of the gate, (2) the phosphorus SSD was driven during the epi growth itself and not by RTA, producing a significantly higher sheet resistance in the SDEs, and (3) the channel doping (in-situ boron) was difficult to control precisely and it ended up much higher ($N_A = 3.5 \times 10^{18}$/cm^3) than intended. The core VRG process has now been improved to eliminate all of these problems. The VRG-pMOS described below were fabricated with this improved core process.

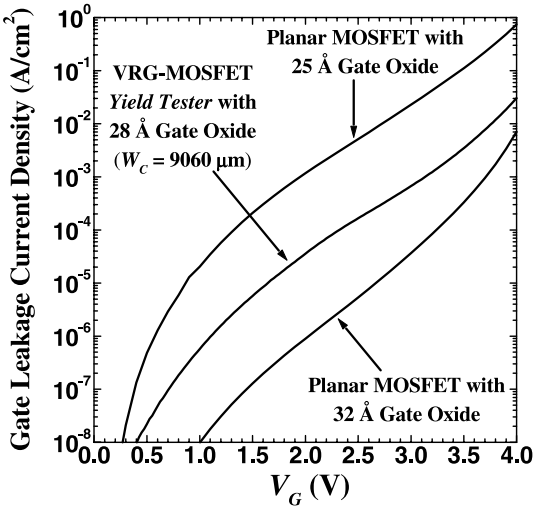

Fig. 16. Comparison of the gate leakage current of a very wide $L_G = 200$ nm VRG yield tester to that of a planar MOSFET. In terms of gate leakage, VRG-MOSFET gate oxides can be scaled well below 28 Å.

Fig. 16 illustrates that the gate leakage current density for a VRG-MOSFET yield tester ($W_C = 9060$ μm) is comparable to that of a planar MOSFET with the same t_{OX}. This suggests that in terms of the gate leakage current, VRG-MOSFET gate oxides can be shrunk well below 28 Å.

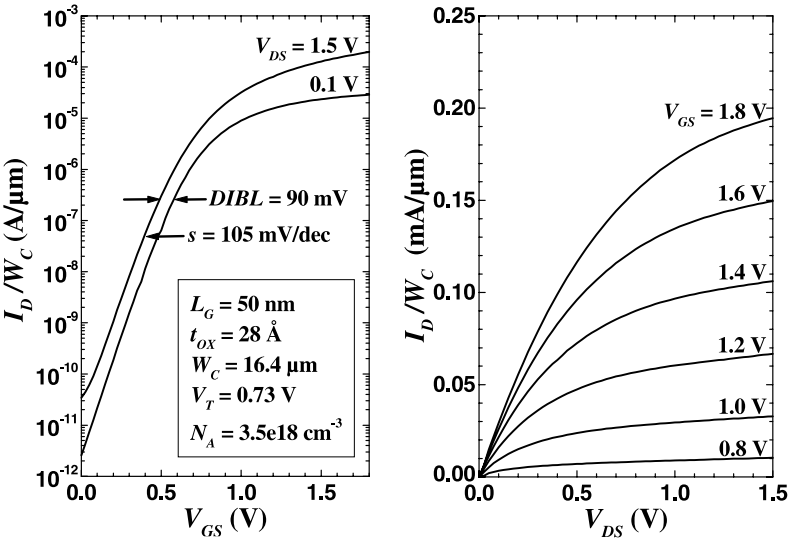

Fig. 15. Subthreshold and I_D–V_{DS} characteristics of a rectangular, $L_G = 50$ nm VRG-nMOSFET with a 28 Å gate oxide. Although this device exhibits respectable short-channel performance, its drive current is relatively low. This is due to several process related problems (see text) that have been eliminated for the more mature pMOSFETs described below.

6. VRG-pMOS device fabrication

We recently demonstrated the first p-channel VRG-MOSFETs [13]. Before and during the fabrication of these pMOS devices, we significantly improved the core VRG process. We have: (1) reduced the thermal budget for the channel growth step to 800 °C (allowing us to subsequently drive SSD by RTA), (2) improved gate oxide processing to provide a uniform, thin oxide over the length of the channel, and (3) improved the SDE engineering. *These improvements enable the fabrication of high-performance short-channel VRG-MOSFETs.* In addition to these improvements, our VRG-pMOSFETs add: (1) channel doping by ion implantation [a critical enabler for VRG-CMOS [12], precise V_T control, and vertical channel engineering], (2) raised SDEs (in contrast to the more conventional raised deep source/drain) for improved overall performance, and (3) a self-aligned recessed-channel structure.

The improved core process used to realize our VRG-pMOSFETs is shown in Fig. 17. This new flow is essentially a subset of a VRG CMOS flow that we envision [12]. A multilayer stack of BSG/nitride/undoped oxide/nitride/BSG/nitride was deposited on top of a boron-doped source layer and a trench was etched through the entire stack. A well-controlled etch in 200:1 HF was used to create 150 or 250 Å recesses in the BSG layers, leading to raised SDEs in the final structure. An *undoped* epitaxial Si device channel was grown selectively in this trench. Excellent crystalline quality, selectivity, and reproducibility were achieved by careful surface preparation to remove trench etch damage, surface contaminants, and native oxide. There was negligible SSD during this 800 °C growth step. After the channel was planarized to the top nitride layer by CMP, the device channel was uniformly doped by a series of phosphorus implants. A subsequent RTA with a negligible thermal budget prevented potentially disastrous transient-enhanced diffusion during the subsequent deposition steps. An a-Si drain landing pad was deposited, implanted with boron, and covered with nitride. A RTA was carried out at 1050 °C to form the SDEs. Note that

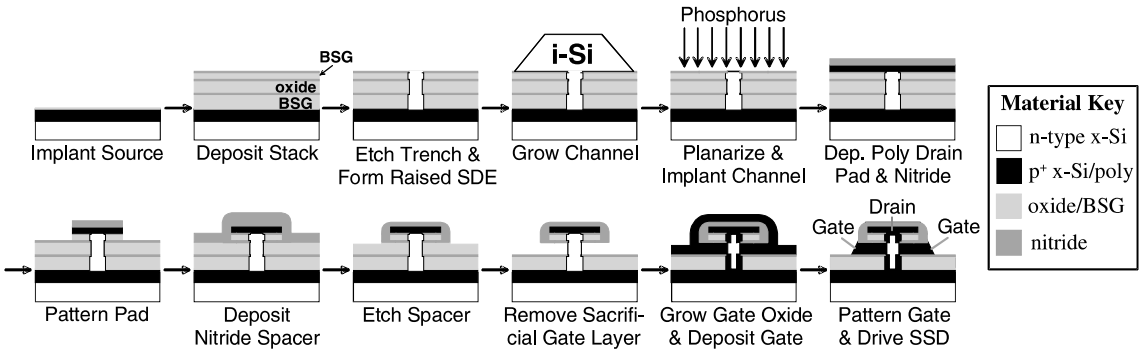

Fig. 17. Detailed description of the VRG-pMOSFET front-end process flow incorporating channel doping by ion implantation and elevated source/drain *extensions*.

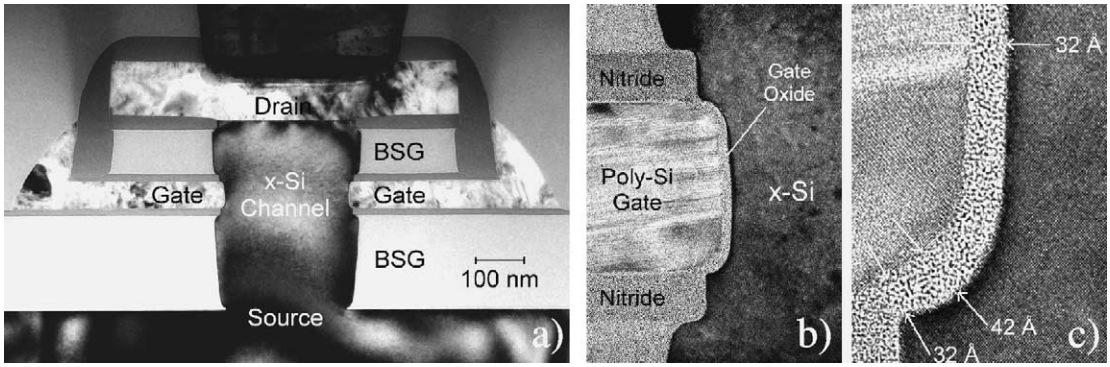

Fig. 18. (a) TEM image of a completed 50 nm VRG-pMOSFET showing perfect crystal quality in the channel, elevated SDEs, and gates on either side of the channel. (b) Blow-up of the active area of the device showing the two nitride offset spacers and a recessed-channel structure. (c) Blow-up of the corner of the gate showing a 32 Å gate oxide without thinning near the gate edges.

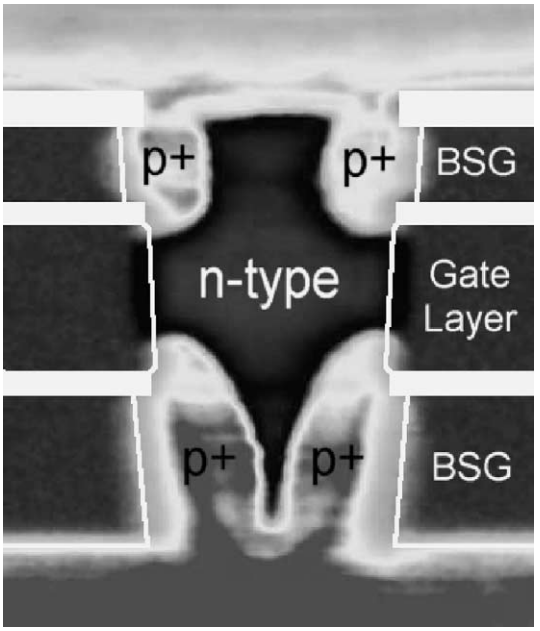

Fig. 19. Scanning capacitance image of a 200 nm VRG-pMOSFET showing the qualitative 2D doping geometry and the n-type channel formed by phosphorus implantation.

this RTA was performed before gate oxidation to prevent boron penetration and to enable the possible future use of high-temperature intolerant, alternative gate stacks. The top of the device was patterned and a nitride spacer was formed to completely encapsulate the landing pad and the top BSG dopant source. The sacrificial oxide layer was then removed selectively. A thin, uniform, wet gate oxide was grown on the channel, and an in-situ boron doped, highly conformal a-Si gate was deposited and recrystallized. The gate was patterned and backend processing was carried out.

The TEM image of Fig. 18(a) shows a completed 50 nm VRG-pMOSFET with an epi-Si channel exhibiting perfect crystal quality and a 32 Å (measured by TEM) gate oxide. This image also illustrates a self-aligned, recessed channel created before gate oxidation and the raised SDEs. Figs. 18(b) and (c) show blow-ups of the active region and the 32 Å gate oxide. The gate oxide does not show the thinning near the edges of the gate that was seen for the initial VRG-nMOS of Fig. 10. The scanning capacitance image of Fig. 19 qualitatively illustrates the doping geometry in a 200 nm VRG-pMOSFET. The extraction of quantitative information about channel lengths and junction depths from images like this is an area of active research.

7. VRG-pMOS device performance

The subthreshold and I_D–V_{DS} characteristics for a VRG-pMOSFET with $L_G = 200$ nm and $t_{OX} = 30$ Å (TEM) are shown in Fig. 20. At an operating voltage of 1.8 V, the drive current of this device divided by its coded width W_C is 550 μA/μm with $I_{OFF} = 2$ nA/μm and subthreshold swing $s = 84$ mV/decade. The associated I_D–V_{DS} characteristics are well-behaved and show floating-body (kink) effects similar to partially depleted SOI. The 100 nm VRG-pMOSFET of Fig. 21 has a very high drive current of 615 μA/μm at 1.5 V with $I_{OFF} = 8$ nA/μm (the 1999 ITRS Roadmap value for 1.5 V

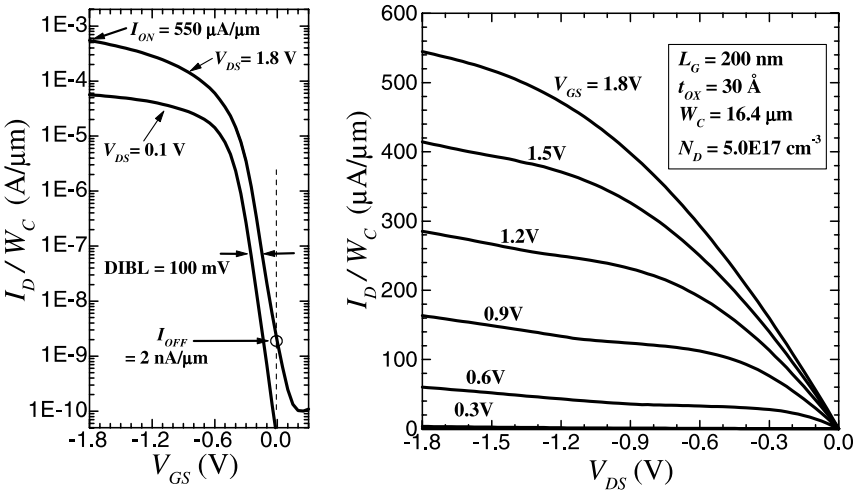

Fig. 20. Subthreshold and I_D–V_{DS} characteristics for a representative $L_G = 200$ nm VRG-pMOSFET with $V_{DD} = 1.8$ V. These data are normalized to the coded width W_C (the device perimeter is ≈2 W_C). With an $I_{OFF} = 2$ nA/μm at $V_{GS} = 0$ V and $V_{DS} = 1.8$ V, the drive current is 550 μA/μm at $V_{GS} = V_{DS} = 1.8$ V.

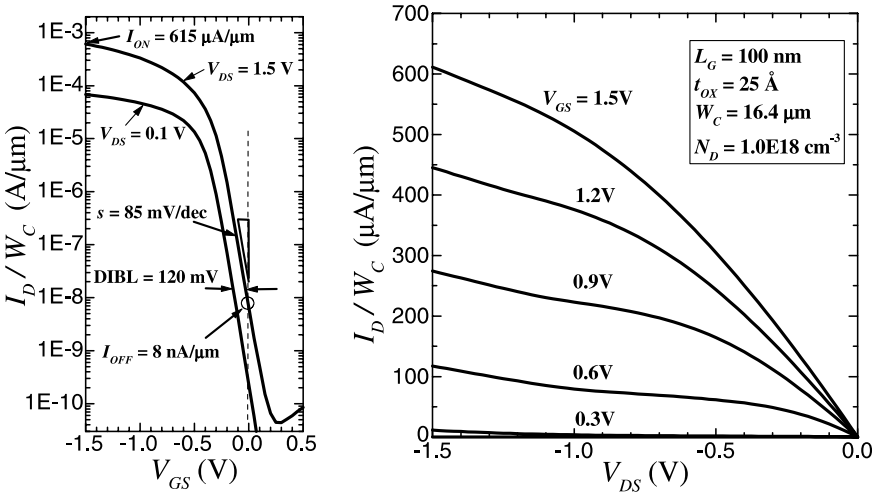

Fig. 21. Subthreshold and I_D–V_{DS} characteristics for a representative $L_G = 100$ nm VRG-pMOSFET with $V_{DD} = 1.5$ V. This device has a 1.5 V roadmap target I_{OFF} of 8 nA/μm with a very high drive current of 615 μA/μm.

high-performance operation). The subthreshold swing $s = 85$ mV/decade. Fig. 22 shows the I_{ON}–I_{OFF} distribution for $L_G \approx 100$ nm pMOSFETs with two different channel doping values along with the roadmap I_{ON}–I_{OFF} specification for high-performance 1.5 V devices. Despite their conservative 25 Å (TEM) gate oxides, our 100 nm pMOSFETs outdrive this specification by nearly 80%. Fig. 23 shows the subthreshold and I_D–V_{DS} characteristics for a 50 nm VRG-pMOSFET with $t_{OX} = 25$ Å and $V_{DD} = 1.0$ V. This device exhibits excellent overall 1.0 V performance with $s = 98$ mV/decade, $I_{ON} = 330$ μA/μm and $I_{OFF} \approx 20$ nA/μm. Fig. 24 indicates that the I_{ON}–I_{OFF} distribution for $L_G \approx 50$ nm VRG-pMOSFETs approaches the 1.0 V roadmap specification without the need for a hyperthin (<20 Å) gate oxide. This respectable 1.0 V performance can be significantly improved by decreasing t_{OX}, incorporating thinner nitride offset spacers (i.e. moving the BSG dopant sources closer to the gate), optimizing the SDE profile and depth, improving the Si surface roughness left behind by the removal of the sacrificial gate layer, and by decreasing the lengths of the SDEs.

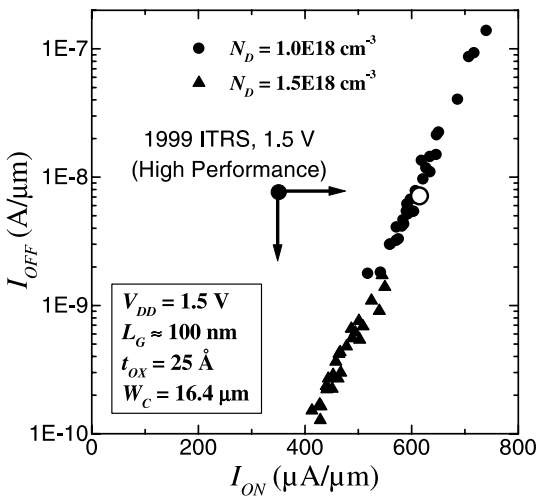

Fig. 22. I_{ON}–I_{OFF} trend for a set of $L_G \approx 100$ nm devices far exceeds the 1999 ITRS target for 1.5 V operation. The device of Fig. 21 is indicated by the open circle.

8. Future options

We have chosen to operate in the partially depleted (PD) regime since this does not require advanced lithography nor is it sensitive to channel thickness variations. PD operation is appropriate as long as it allows continued performance improvement through scaling. Although conventional halos, super-halos, and super-steep retrograde wells are difficult to implement in the VRG process, their absence can be offset by very tight ($3\sigma < 3\%$) L_G control. The new knob of vertical channel engineering (i.e. grading the channel doping along its length) may be used to improve short-channel performance and enhance the surface mobility. Although the VRG process is mechanically scalable to sub-30 nm gate lengths with excellent control, for ULSI applications it will be difficult to maintain PD operation and provide electrical scalability to gate lengths this short. However, if one provides a very thin silicon channel (t_{Si}) by advanced lithography or other means, then the VRG process provides a new route to the fabrication of highly

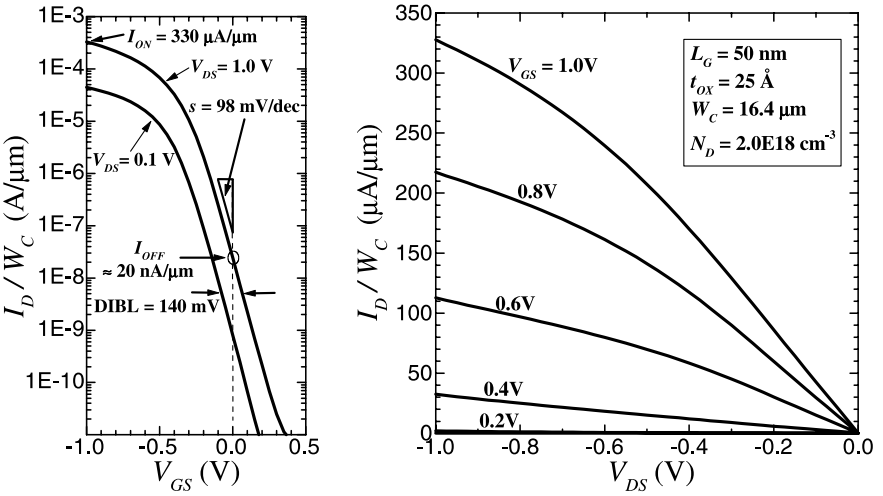

Fig. 23. Subthreshold and I_D–V_{DS} characteristics for a representative $L_G = 50$ nm VRG-pMOSFET with $V_{DD} = 1.0$ V. With an I_{OFF} of about 20 nA/μm, this device drives 330 μA/μm. This device was fabricated without advanced lithography using production tools, techniques, and materials.

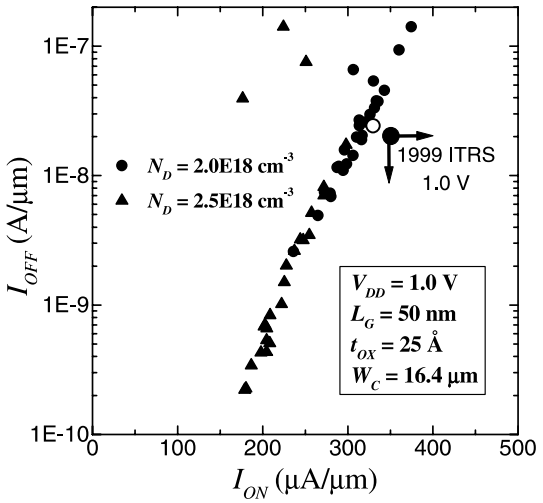

Fig. 24. I_{ON}–I_{OFF} trend for a set of $L_G \approx 50$ nm devices approaches the 1999 ITRS target for 1.0 V operation, even with a relatively thick 25 Å (TEM) gate oxide. The device of Fig. 23 is indicated by the open circle.

scalable, fully depleted double-gate MOSFETs with self-aligned gates and well-controlled parasitics.

9. Side-by-side VRG CMOS

In Ref. [12], we describe a process for integrating n-channel and p-channel VRG-MOSFETs to form side-by-side CMOS. This process achieves all doping by masked ion implantation, except for the gate electrodes and, of course, the SDEs. The gate electrodes are deposited as in situ doped, conformal, n- and p-polysilicon films in two separate modules. In each of these modules, the sacrificial gate layer is removed, the gate oxide is grown, and the n- or p-polysilicon gate is deposited. With a straightforward no-additional-mask modification of the VRG process, one can eliminate floating-body effects by incorporating regional body ties (as in conventional bulk CMOS) through the base of each device pillar. The top and bottom source/drain as well as the gate can be salicided. The complete flow has only three more lithographic steps than planar CMOS. We have done a detailed comparison of several standard library cells laid out for VRG and for conventional planar technology. Assuming equivalent lithographic design rules, we find comparable density for random logic, because both are limited primarily by lithographic constraints. Significant improvements in packing density may be possible for VRG CMOS in dense, regular circuits, or in circuits that benefit from decoupling the gate length from the cell area. However, for the same packing density, the current drive can be nearly doubled because both sides of the device pillar drive in parallel (the data of Fig. 22 indicate an 80% enhancement). Since the gate capacitance also doubles, this could dramatically increase the speed of circuits that have a significant interconnect load. Even gate-loaded circuits benefit from SOI-like reduction of substrate capacitance, together with overlap capacitances competitive with current planar MOSFETs, as shown in Ref. [12]. The primary barriers to the adoption of VRG CMOS in ULSI applications will be the well-founded conservatism of manufacturing when faced with the yield and reliability risks of a substantially new process.

10. Conclusions

We have demonstrated both n- and p-channel versions of a new MOSFET intended for high-performance logic and memory applications in which: (1) all critical dimensions are controlled precisely without lithography and dry etch, (2) the channel is self-aligned to the gate, and (3) a high-quality gate oxide is grown on a single-crystal Si channel. Using current manufacturing methods, materials, and tools, the unique VRG process enables the fabrication of high-performance 50 nm devices with ultrathin gate oxides, precise L_G control, raised SDEs, and SOI-like parasitics. Our 100 nm pMOSFETs far exceed the 1.5 V roadmap I_{ON}–I_{OFF} targets, and our 50 nm VRG-pMOSFETs with $t_{OX} = 25$ Å approach the 1.0 V roadmap target of $I_{ON} = 350$ μA/μm at $I_{OFF} = 20$ nA/μm without the need for a hyperthin (<20 Å) gate oxide. We believe that the VRG process can be integrated in a complementary logic that is competitive in density and process complexity with traditional planar CMOS while providing precise control of all critical transistor dimensions without lithography, enhanced performance in circuits with a significant interconnect load, and entirely new opportunities for the continued scaling of the Si MOSFET.

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